MC10H145

16 x 4 Bit Register File (RAM)

The MC10H145 is a 16 x 4 bit register file. The active-low chip select allows easy expansion.

The operating mode of the register file is controlled by the $\overline{WE}$ input. When $\overline{WE}$ is "low" the device is in the write mode, the outputs are "low" and the data present at D_n input is stored at the selected address, when $\overline{WE}$ is "high," the device is in the read mode – the data state at the selected location is present at the Q_n outputs.
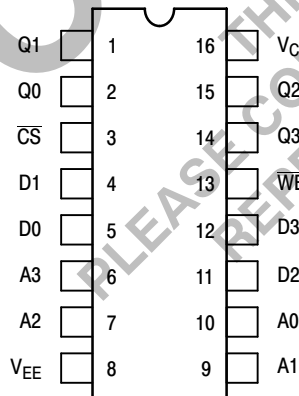
- Address Access Time, 4.5 ns Typical
- Power Dissipation, 700 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_n	Q_n
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	X	Q
Disabled	H	X	X	L

Q-State of Addressed Cell

DIP PIN ASSIGNMENT

Q1	1	16	V_{CC}
Q0	2	15	Q2
$\overline{CS}$	3	14	Q3
D1	4	13	$\overline{WE}$
D0	5	12	D3
A3	6	11	D2
A2	7	10	A0
V_{EE}	8	9	A1

Pin assignment is for Dual−in−Line Package.
For PLCC pin assignment, see the Pin Conversion Tables
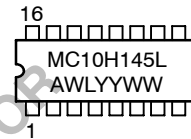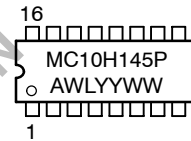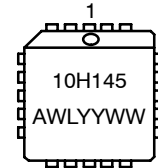on page 6−11 of the Motorola MECL Data Book (DL122/D).

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MARKING DIAGRAMS

CDIP−16
L SUFFIX
CASE 620

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MC10H145L
AWLYYWW
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PDIP−16
P SUFFIX
CASE 648

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MC10H145P
AWLYYWW
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PLCC−20
FN SUFFIX
CASE 775

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10H145
AWLYYWW
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A   = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H145L	CDIP−16	25 Units/Rail
MC10H145P	PDIP−16	25 Units/Rail
MC10H145FN	PLCC−20	xx Units/Rail

MC10H145

BLOCK DIAGRAM
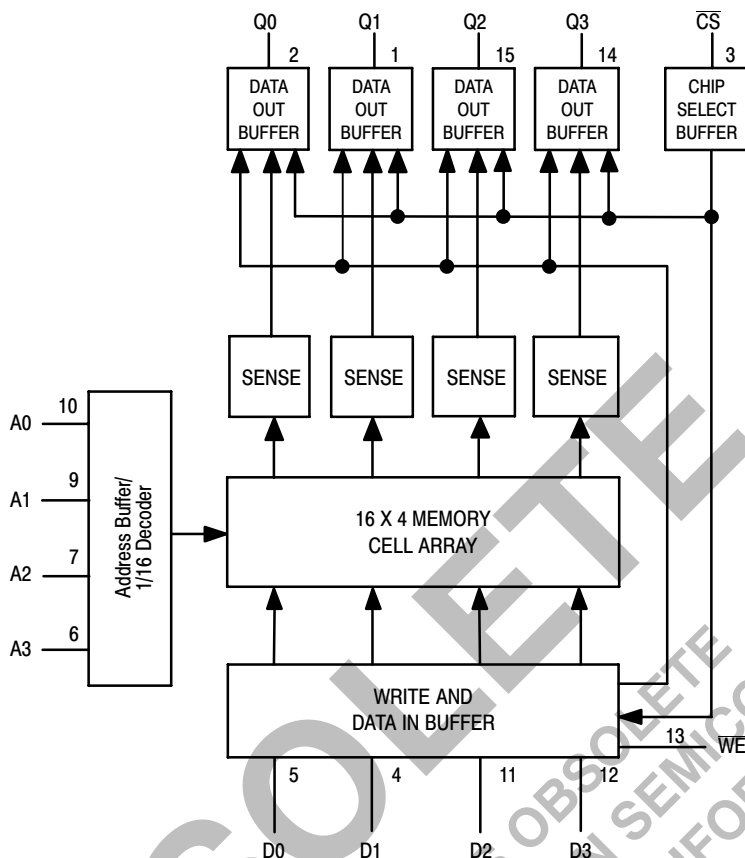
MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current – Continuous – Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range – Plastic – Ceramic	–55 to +150 –55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note)

Symbol	Characteristic	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
I_E	Power Supply Current	–	160	–	163	–	165	mA
I_{inH}	Input Current High	–	375	–	220	–	220	μA
I_{inL}	Input Current Low	0.5	–	0.5	–	0.3	–	μA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts.

AC PARAMETERS

Symbol	Characteristics	MC10H145 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ±5%		Unit	Conditions
		Min	Max		

t_{ACS} t_{RCS} t_{AA}	Read Mode
	  Chip Select Access Time
	  Chip Select Recovery Time
	  Address Access Time
		0
		0
		0
			4.0
			4.0
			6.0
				ns	Measured from 50% of input to 50% of output. See Note 2.

t_W t_{WSD} t_{WHD} t_{WSA} t_{WHA} t_{WSCS} t_{WHCS} t_{WS} t_{WR}	Write Mode
	  Write Pulse Width
	  Data Setup Time Prior to Write
	  Data Hold Time After Write
	  Address Setup Time Prior to Write
	  Address Hold Time After Write
	  Chip Select Setup Time Prior to Write
	  Chip Select Hold Time After Write
	  Write Disable Time
	  Write Recovery Time
		6.0
		0
		1.5
		3.5
		1.5
		0
		1.5
		1.0
		1.0
			–
			–
			–
			–
			–
			–
			–
			4.0
			4.0
				ns	t_{WSA} = 3.5 ns
					Measured at 50% of input to 50% of output. t_W = 6.0 ns.

t_{CSD} t_{CSW} t_{CSA} t_{CHD} t_{CHW} t_{CHA} t_{CS}	Chip Enable Strobe Mode
	  Data Setup Prior to Chip Select
	  Write Enable Setup Prior to Chip Select
	  Address Setup Prior to Chip Select
	  Data Hold Time After Chip Select
	  Write Enable Hold Time After Chip Select
	  Address Hold Time After Chip Select
	  Chip Select Minimum Pulse Width
		0
		0
		0
		1.0
		0
		2.0
		4.0
			–
			–
			–
			–
			–
			–
			–
				ns	Guaranteed but not tested on standard product. See Figure 1.

t_r, t_f	Rise and Fall Time
	  Address to Output
	  CS to Output
		0.6
		0.6
			2.5
			2.5
				ns	Measured between 20% and 80% points.

C_{in} C_{out}	Capacitance
	  Input Capacitance
	  Output Capacitance
		–
		–
			6.0
			8.0
				pF	Measured with a pulse technique.

NOTES:

1. Test circuit characteristics: R_T = 50 Ω, MC10H145. C_L ≤ 5.0 pF (including jig and Stray Capacitance). Delay should be derated 30 ps/pF for capacitive loads up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the worst-case bit in the memory.
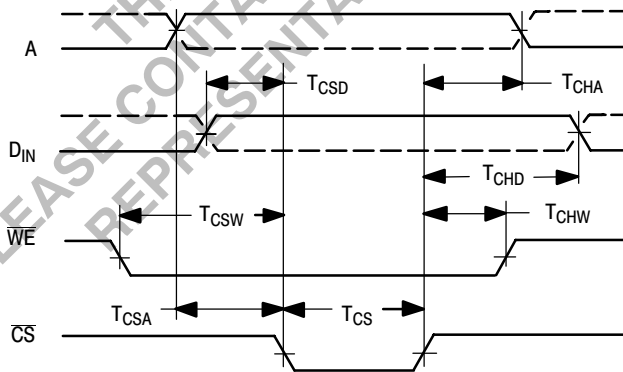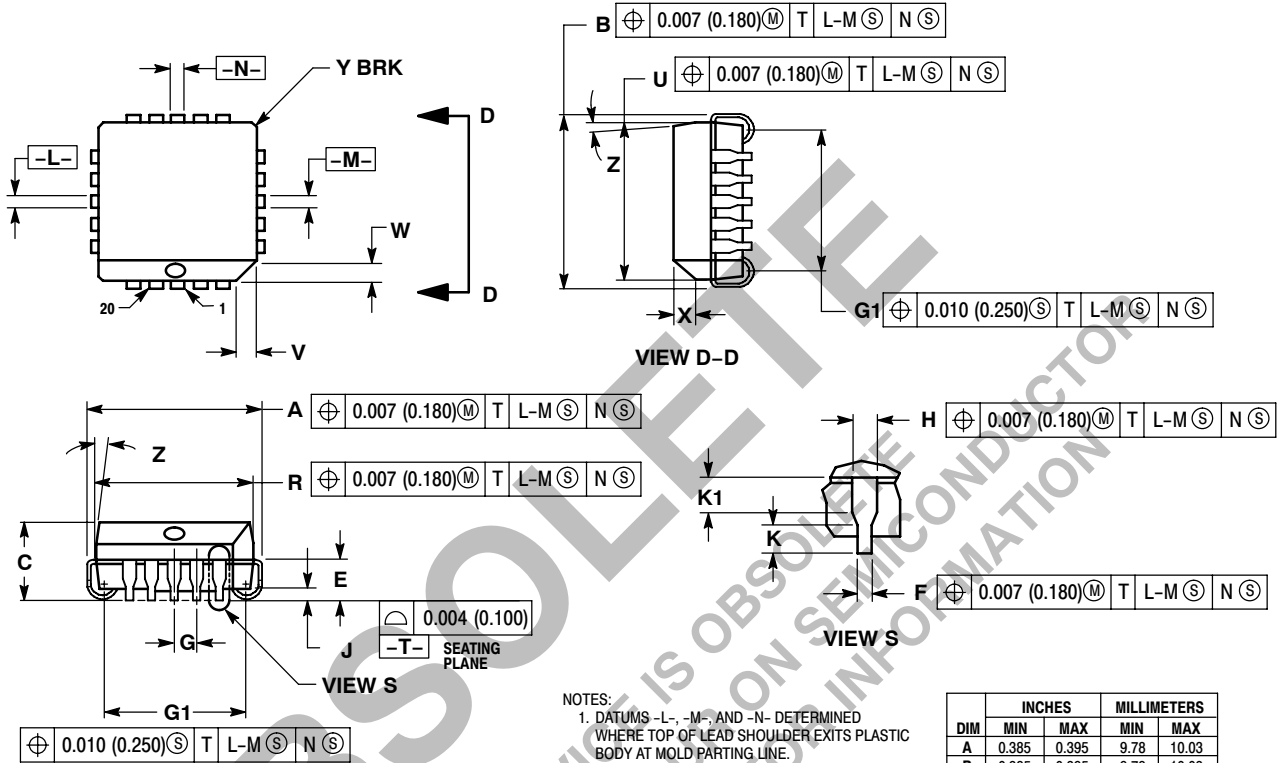3. For proper use of MECL in a system environment, consult MECL System Design Handbook.

Figure 1. Chip Enable Strobe Mode

PACKAGE DIMENSIONS

PLCC–20
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775–02
ISSUE C

B $\oplus$ | 0.007 (0.180)(M) | T | L–M (S) | N (S)

U $\oplus$ | 0.007 (0.180)(M) | T | L–M (S) | N (S)

G1 $\oplus$ | 0.010 (0.250)(S) | T | L–M (S) | N (S)

VIEW D–D

A $\oplus$ | 0.007 (0.180)(M) | T | L–M (S) | N (S)

R $\oplus$ | 0.007 (0.180)(M) | T | L–M (S) | N (S)

H $\oplus$ | 0.007 (0.180)(M) | T | L–M (S) | N (S)

F $\oplus$ | 0.007 (0.180)(M) | T | L–M (S) | N (S)

$\bigtriangleup$ | 0.004 (0.100)

–T– **SEATING PLANE**

VIEW S

$\oplus$ | 0.010 (0.250)(S) | T | L–M (S) | N (S)

NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

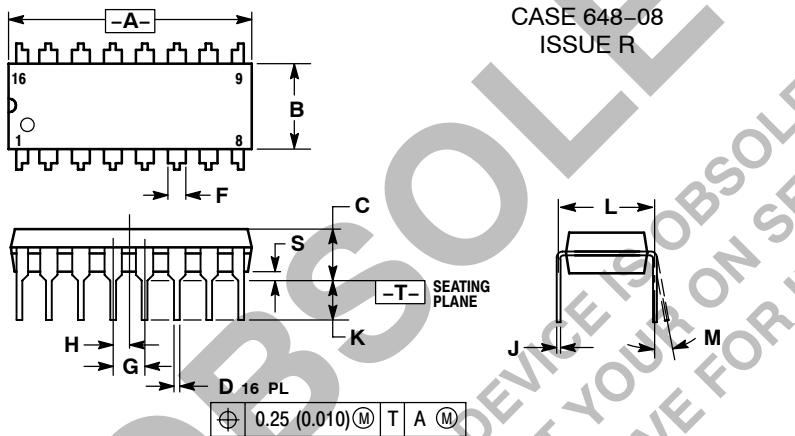| DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

CDIP–16
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE T
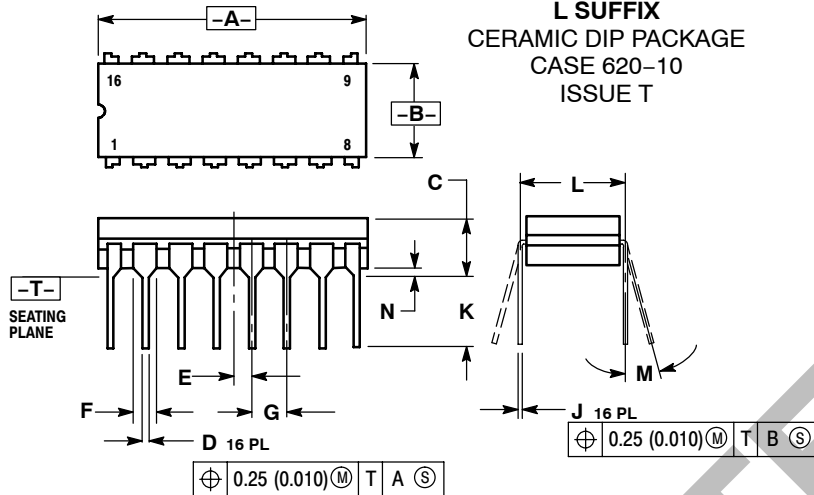
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

⊕ 0.25 (0.010) Ⓜ T A Ⓢ

J 16 PL ⊕ 0.25 (0.010) Ⓜ T B Ⓢ

D 16 PL

PDIP–16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

⊕ 0.25 (0.010) Ⓜ T A Ⓜ

D 16 PL